

FIG. 1

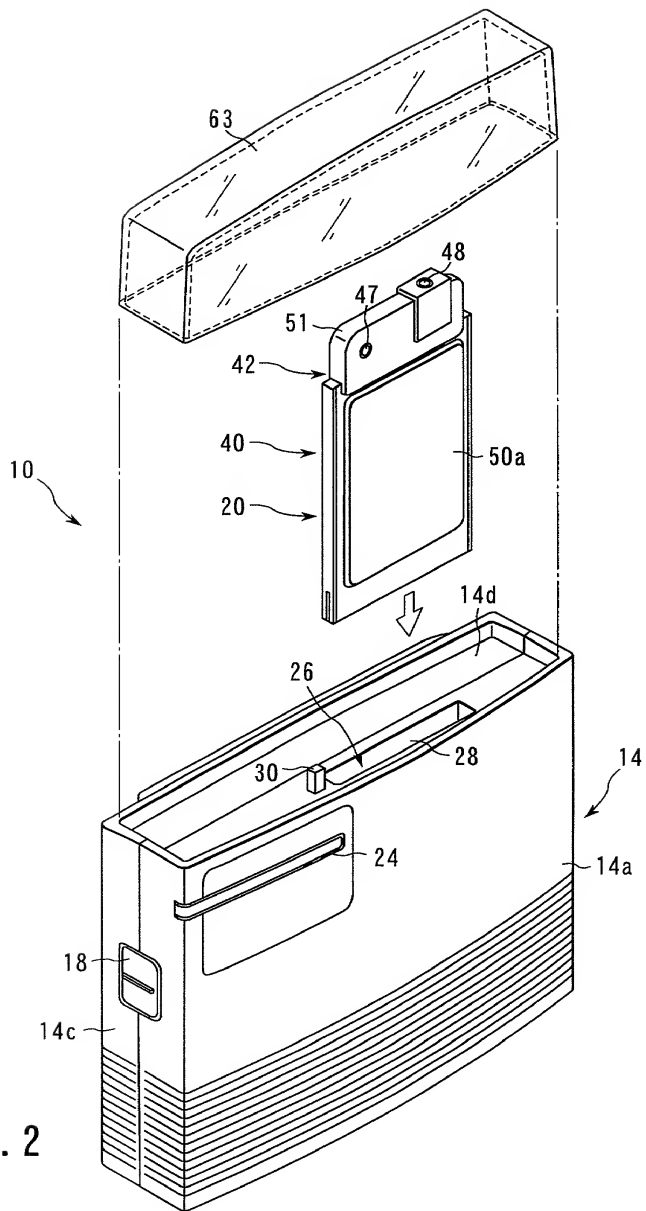


FIG. 2

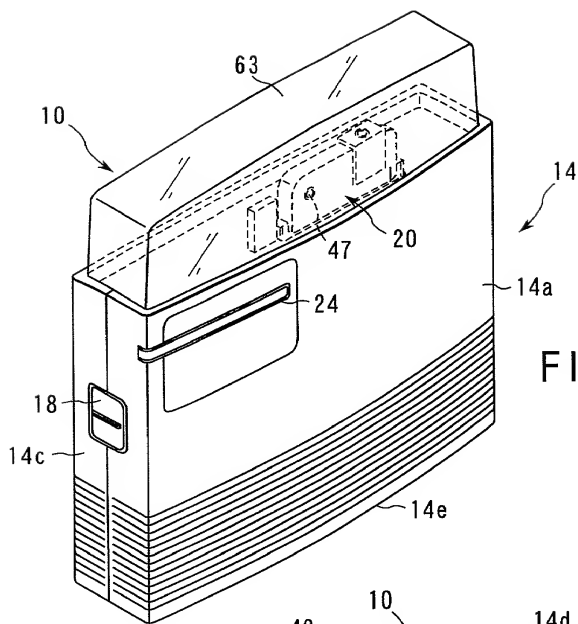


FIG. 3

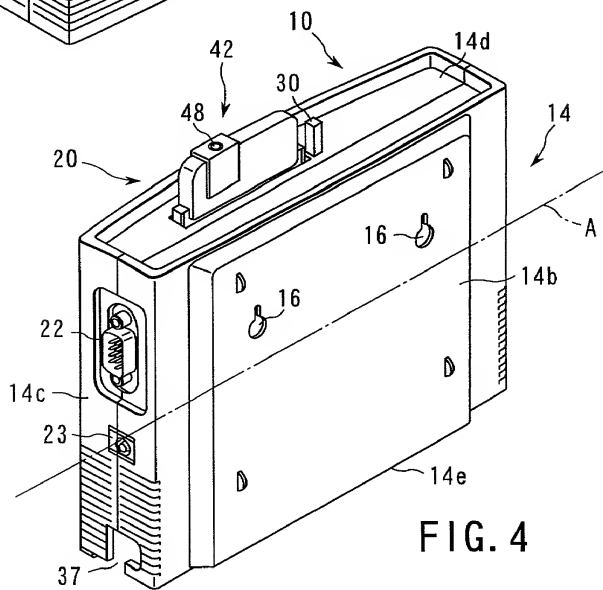


FIG. 4

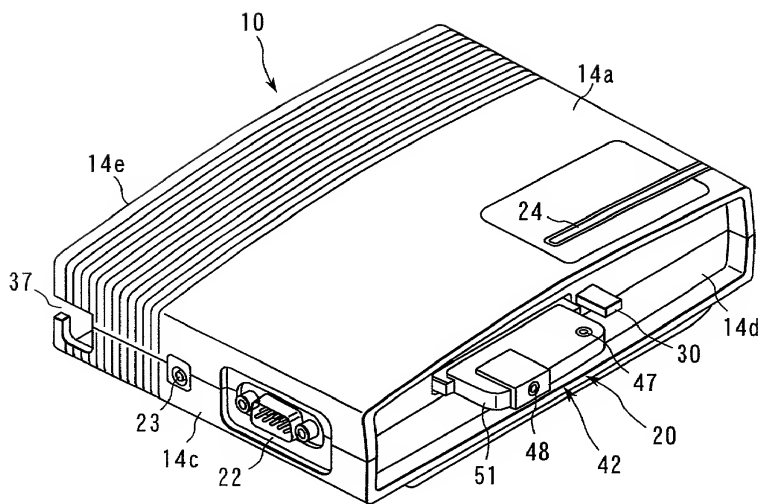


FIG. 5

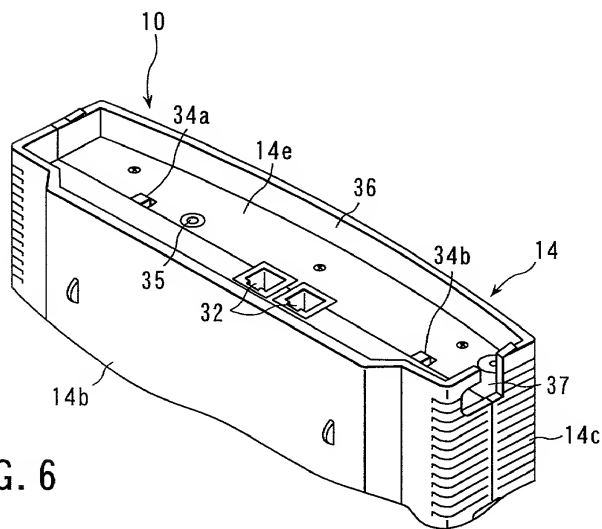
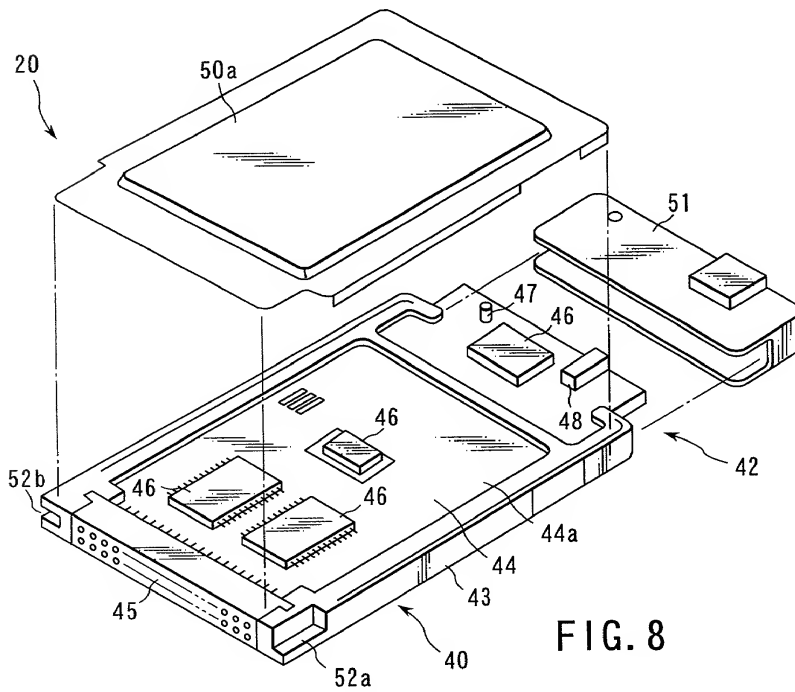
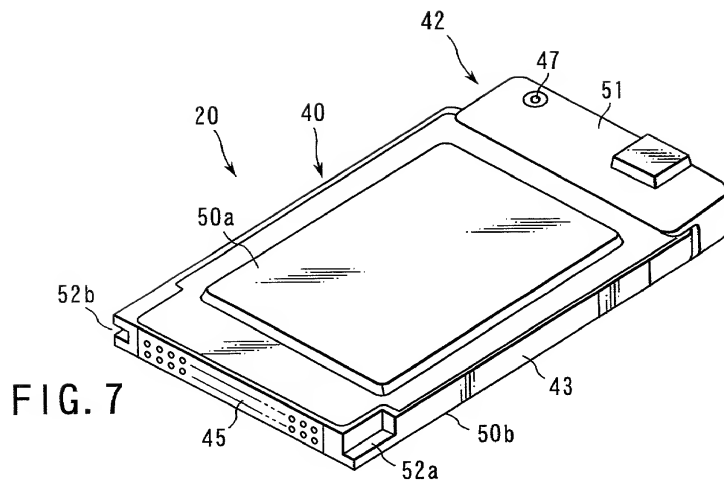


FIG. 6



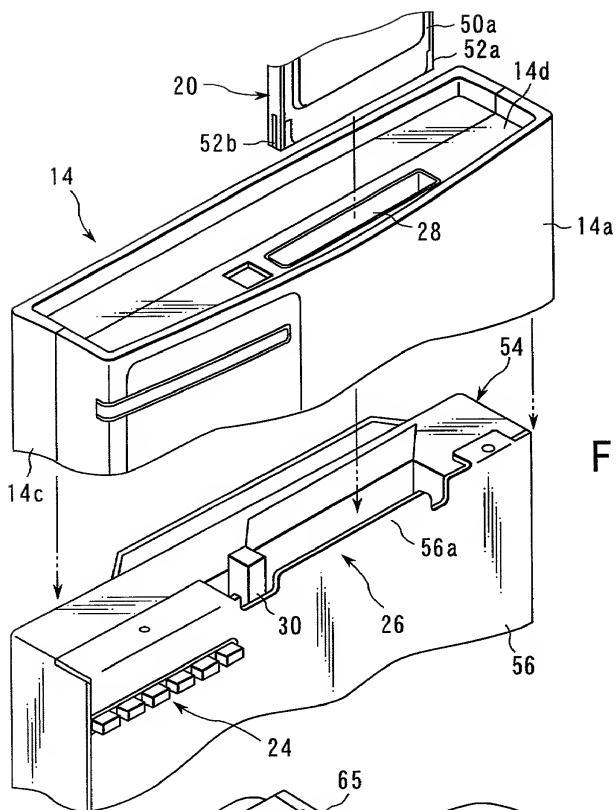


FIG. 9

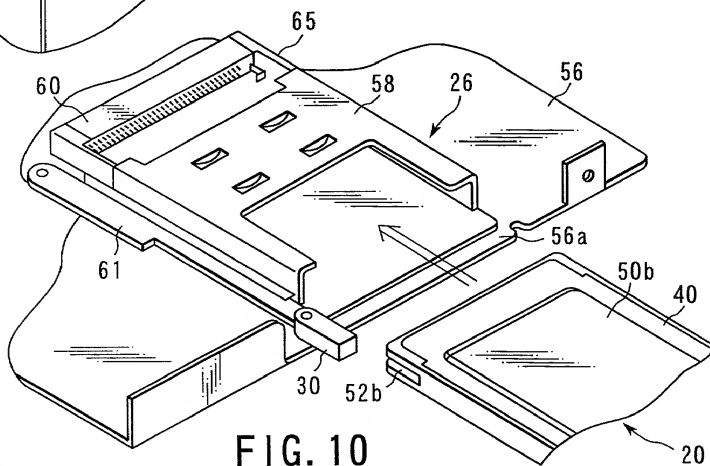


FIG. 10

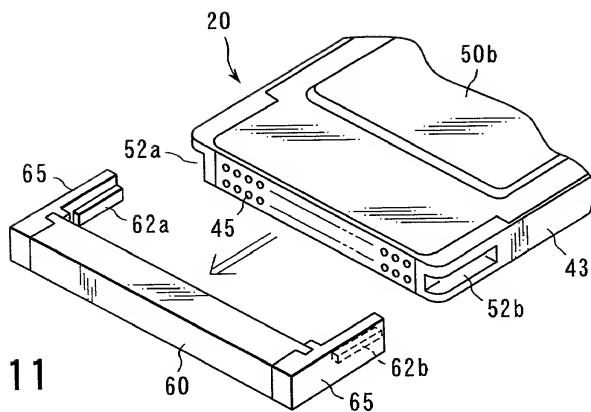


FIG. 11

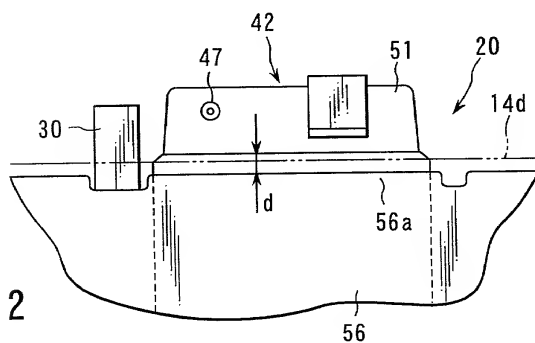


FIG. 12

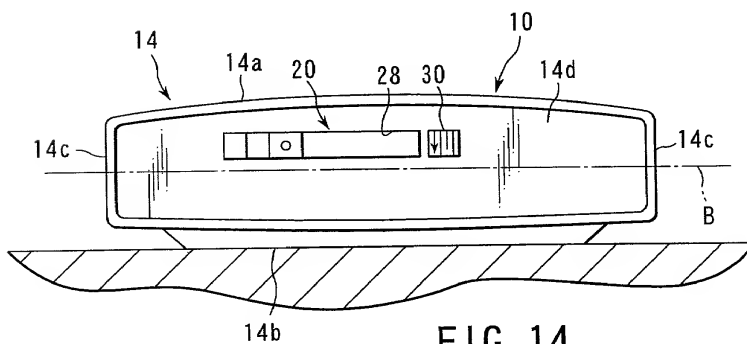


FIG. 14

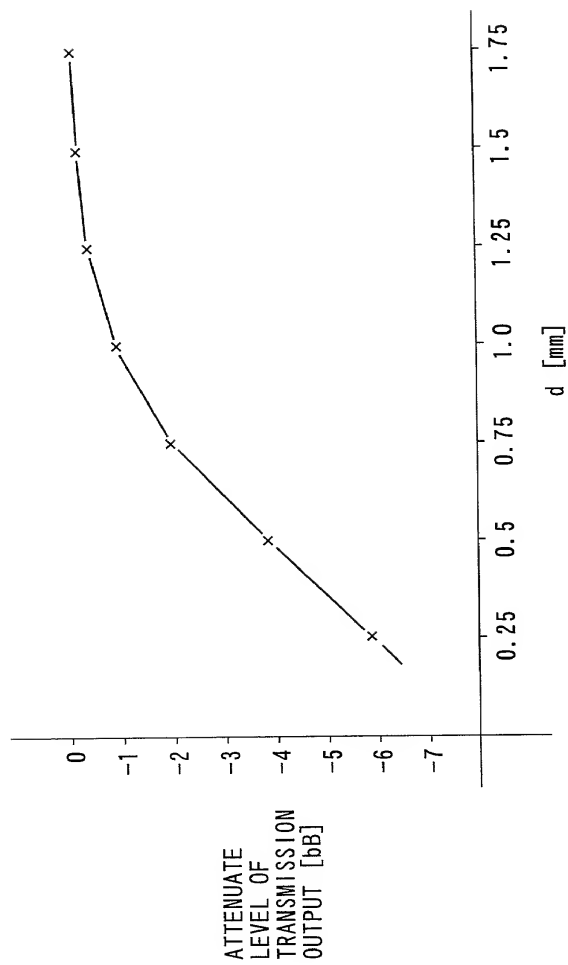


FIG. 13



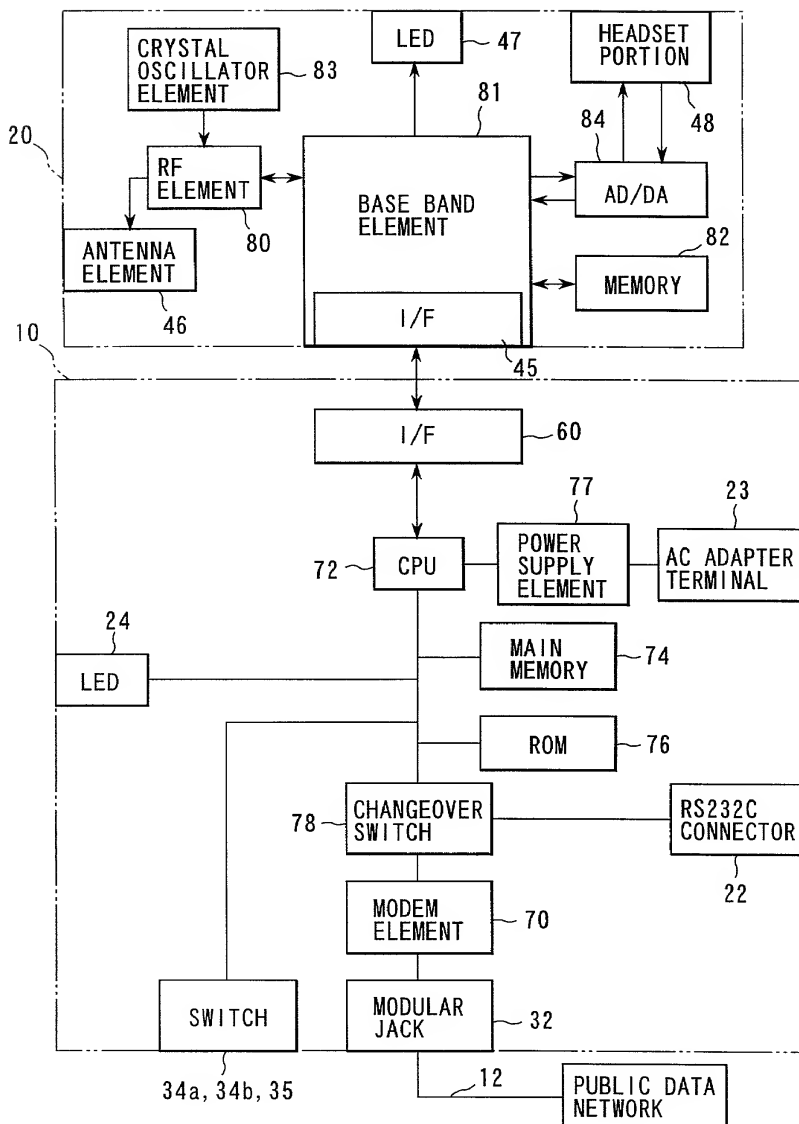


FIG. 15

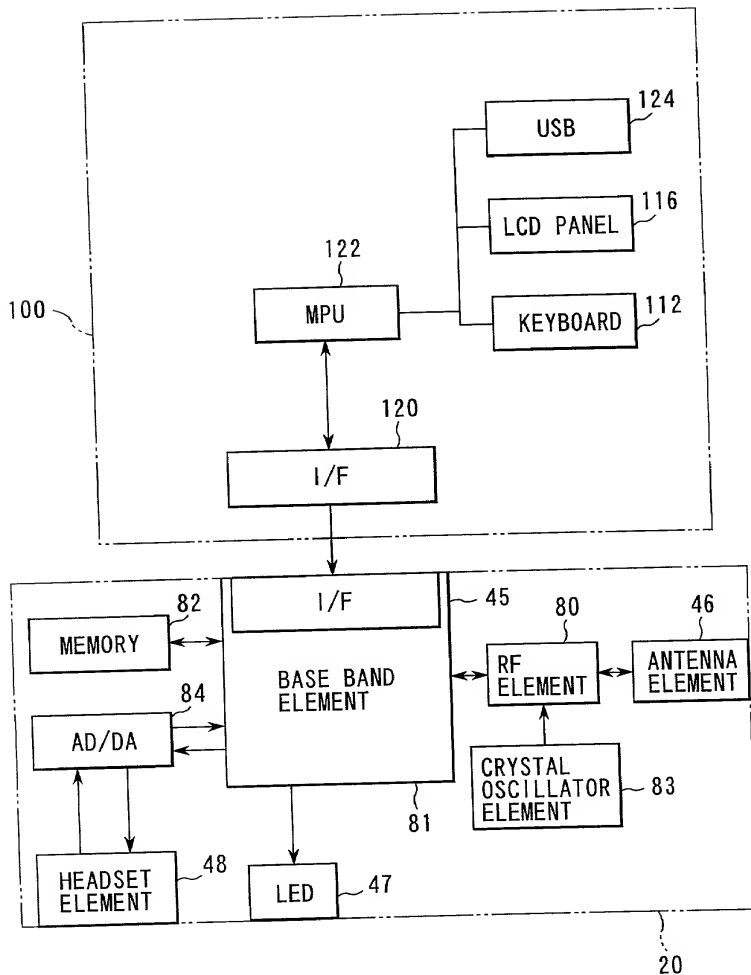


FIG. 16

SETTING OF SLIDE & ROTARY SWITCHES

OPERATING STATES	SLIDE SW1	SLIDE SW2	POs. #	ROTARY SWITCH				REMARKS
				1	2	3	4	
NORMAL (MODEM)	L	L	0, 2, 4, 6	L	x	x	L	
NORMAL (AT)	H	L	0, 2, 4, 6	L	x	x	L	
MAINTENANCE (MODEM)	L	H	0, 2, 4, 6	L	x	x	L	CPU PROHIBITS INTERRUPTION OF UART SYSTEM
MAINTENANCE (CPU)	H	H	0, 2, 4, 6	L	x	x	L	PIN CODE CHANGED
INITIALIZATION 1	L	L	1, 3, 5, 7	H	x	x	L	EEPROM INITIALIZATION EXECUTED
INITIALIZATION 0	H	L	1, 3, 5, 7	H	x	x	L	EEPROM INITIALIZATION STARTED
RESERVED	L	H	1, 3, 5, 7	H	x	x	L	
TEST MODE	H	H	1, 3, 5, 7	H	x	x	L	PCB INSPECTION, CPU F/W RELOADING, ETC.
RESERVED	L	L	8	L	x	x	H	
TCI (HCI)	H	L	8	L	x	x	H	FOR HCI EVALUATION
RESERVED	L	H	8	L	x	x	H	
TCI (L2CAP)	H	H	8	L	x	x	H	L2CAP EVALUATION
RESERVED	L	L	9	H	x	x	H	MODEM-DIR STATE
RESERVED	H	L	9	H	x	x	H	TA STATE
RESERVED	L	H	9	H	x	x	H	MODE STATE
RESERVED	H	H	9	H	x	x	H	TA STATE

USER  
SETTING

SETTING FOR  
MAINTENANCE  
OPERATION

SETTING FOR  
SHIPMENT

FIG. 17